

FIG. 1

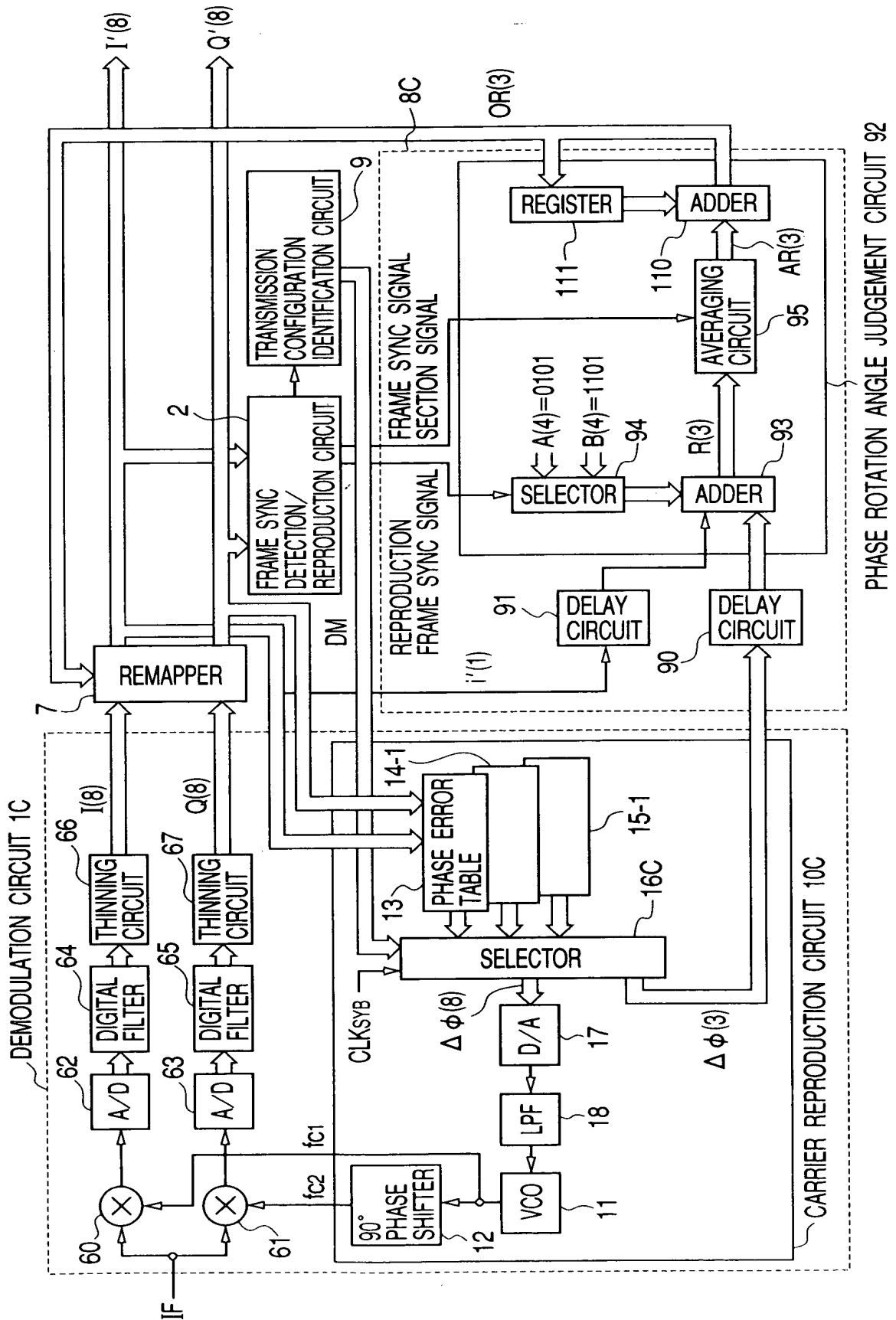


FIG. 2A

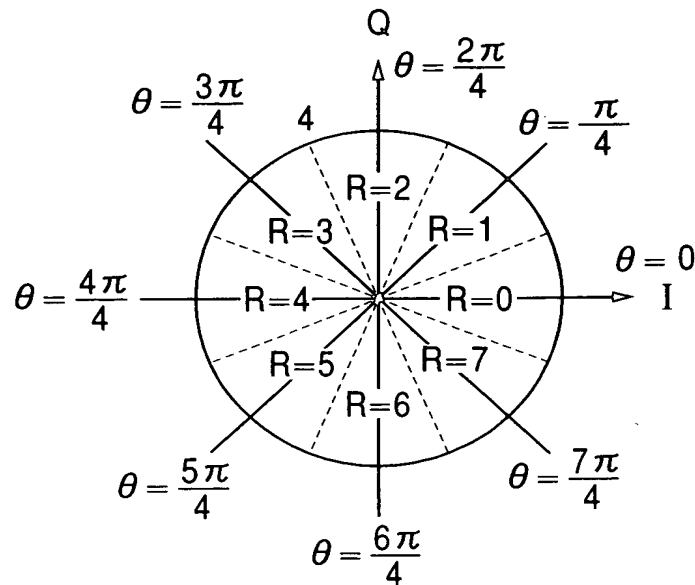


FIG. 2B

θ	R	R(3)
0	0	000
$\pi/4$	1	001
$2\pi/4$	2	010
$3\pi/4$	3	011
$4\pi/4$	4	100
$5\pi/4$	5	101
$6\pi/4$	6	110
$7\pi/4$	7	111

FIG. 3

AVERAGING CIRCUIT 95

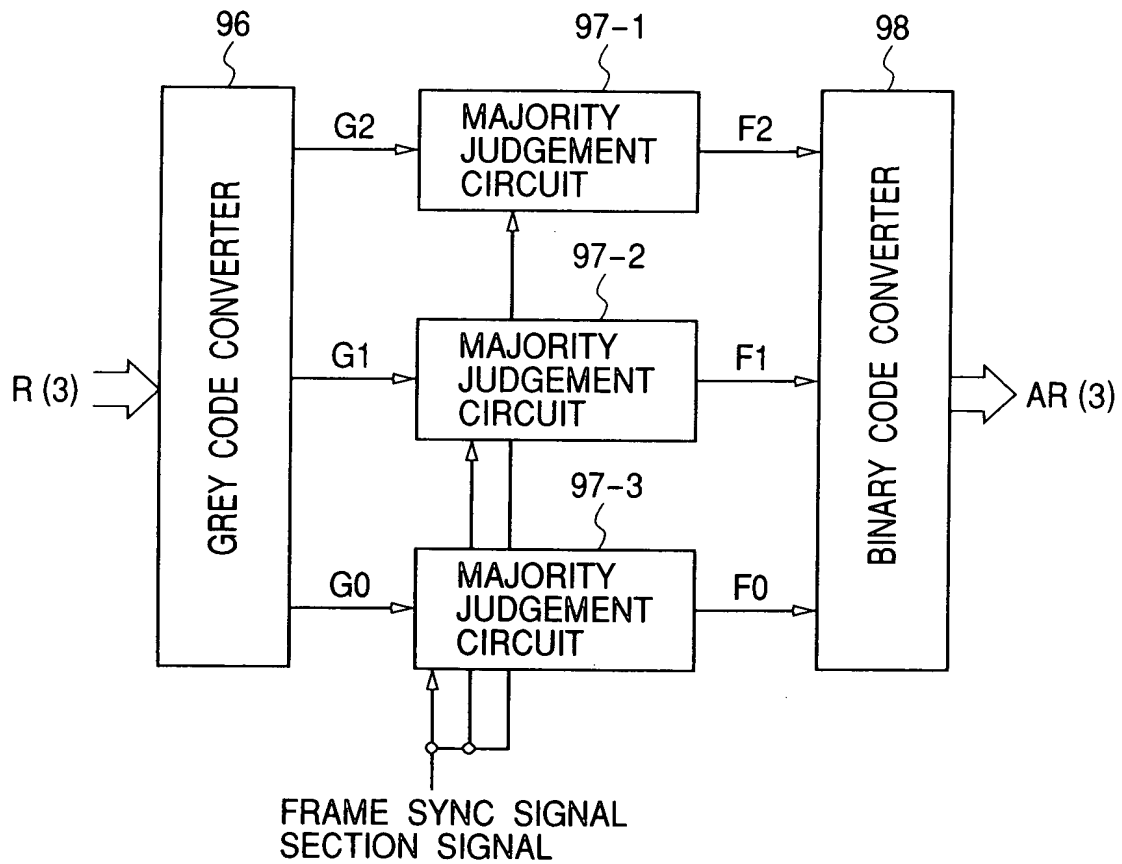


FIG. 4A

INPUT	OUTPUT
0 0 0	0 0 0
0 0 1	0 0 1
0 1 0	0 1 1
0 1 1	0 1 0
1 0 0	1 1 0
1 0 1	1 1 1
1 1 0	1 0 1
1 1 1	1 0 0

FIG. 4B

INPUT	OUTPUT
0 0 0	0 0 0
0 0 1	0 0 1
0 1 1	0 1 0
0 1 0	0 1 1
1 1 0	1 0 0
1 1 1	1 0 1
1 0 1	1 1 0
1 0 0	1 1 1

FIG. 5

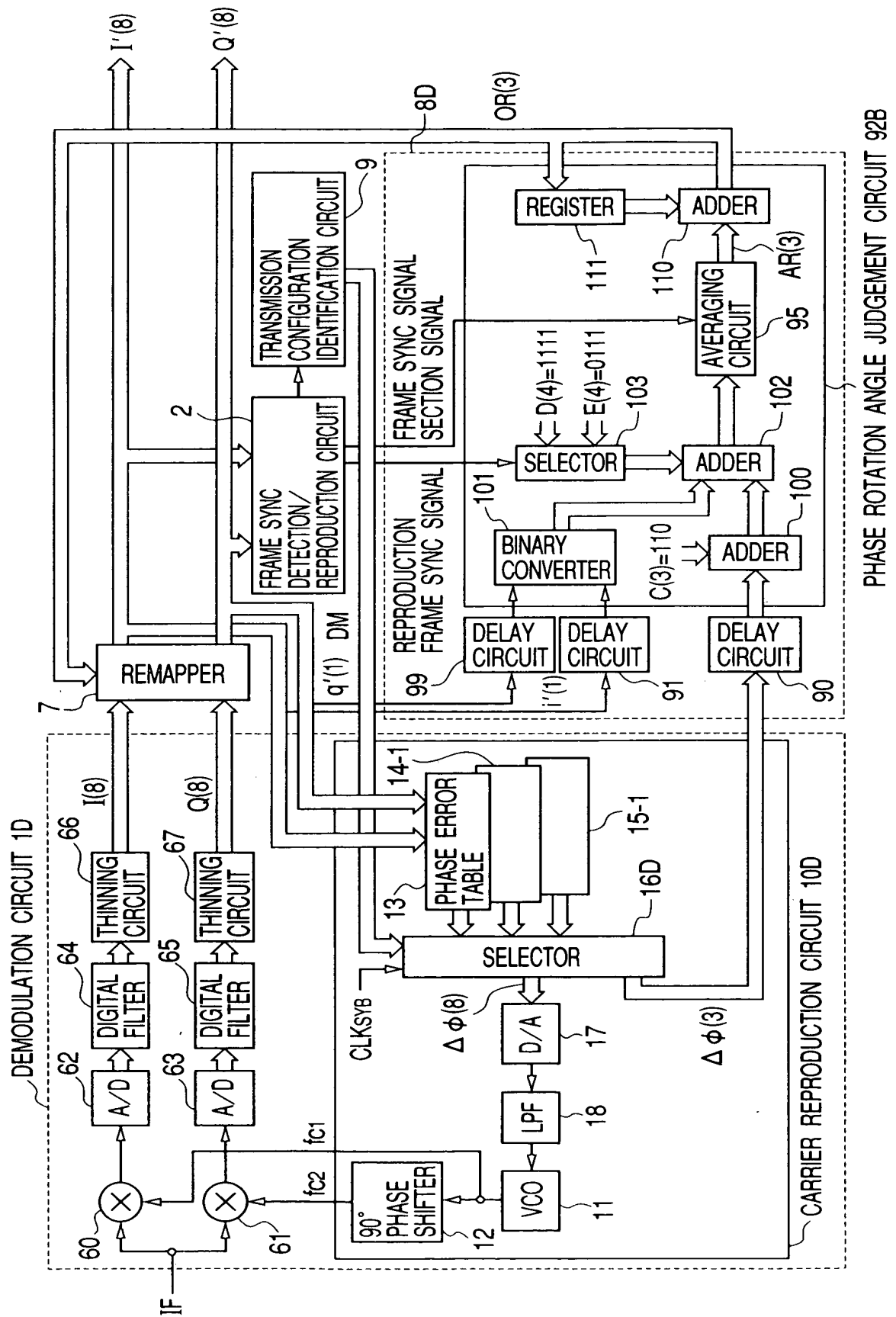
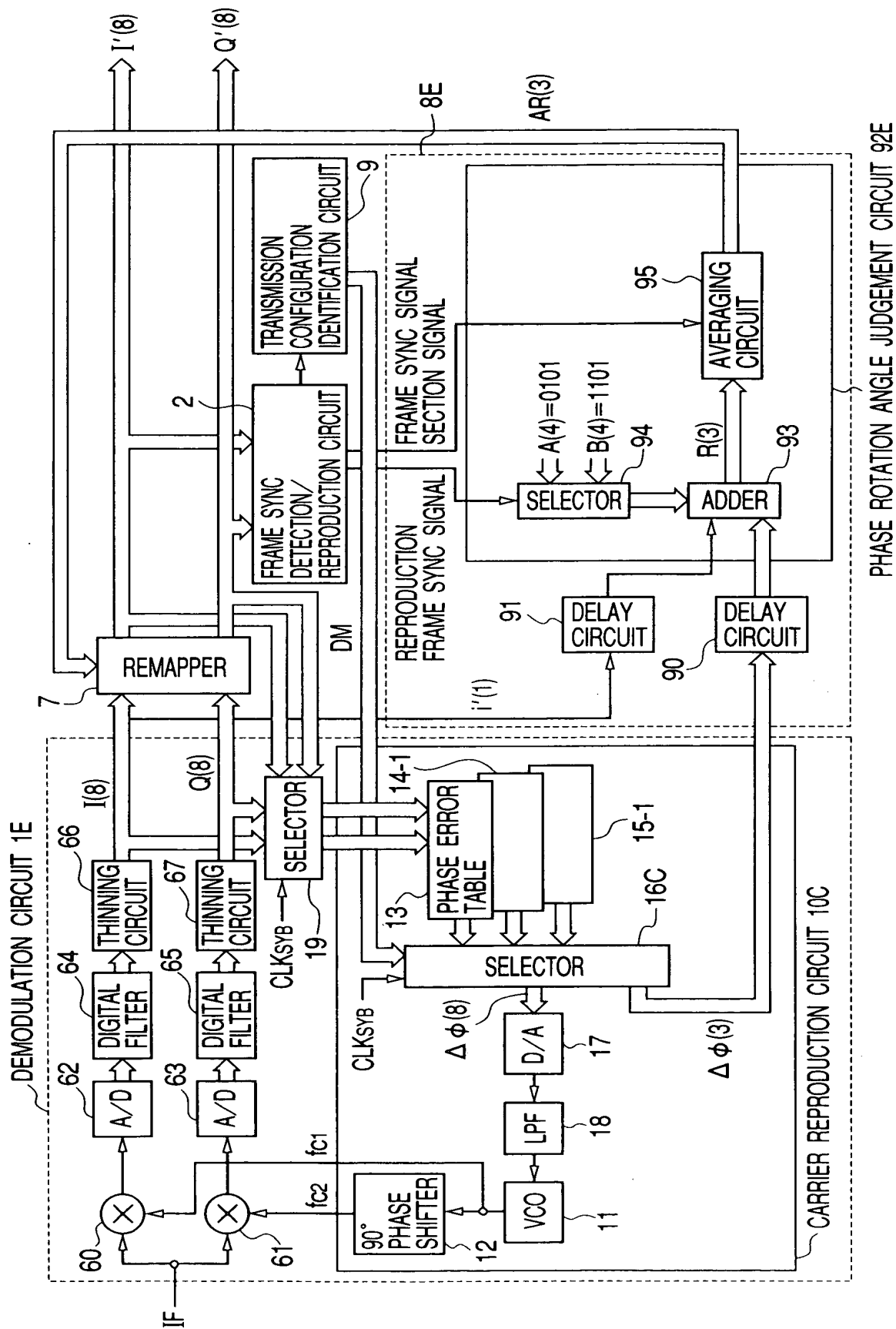


FIG. 6

INPUT (q (1) i (1))	OUTPUT
0 0	0 0
0 1	0 1
1 1	1 0
1 0	1 1

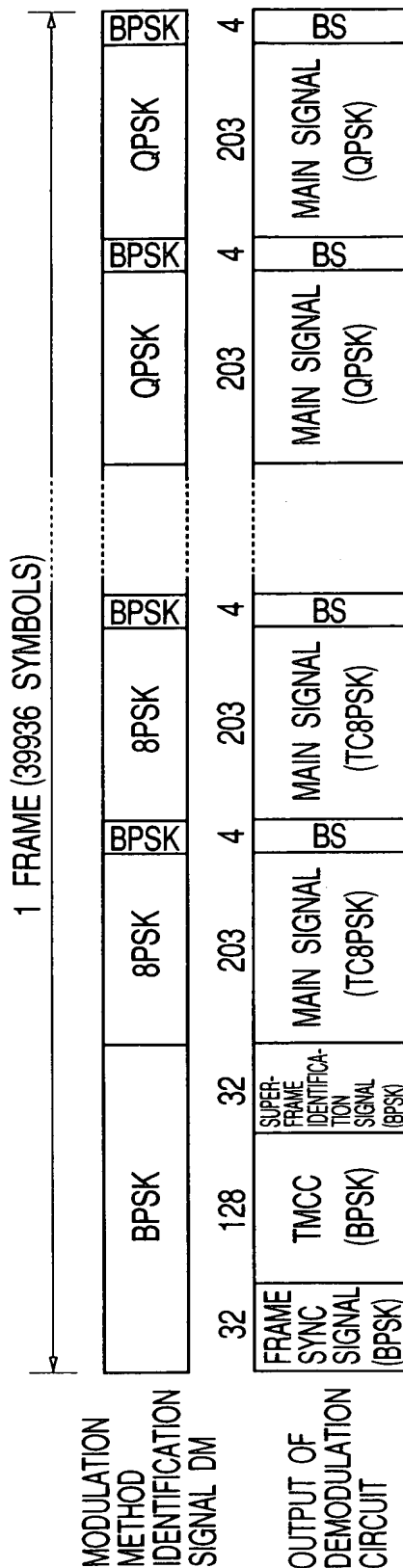
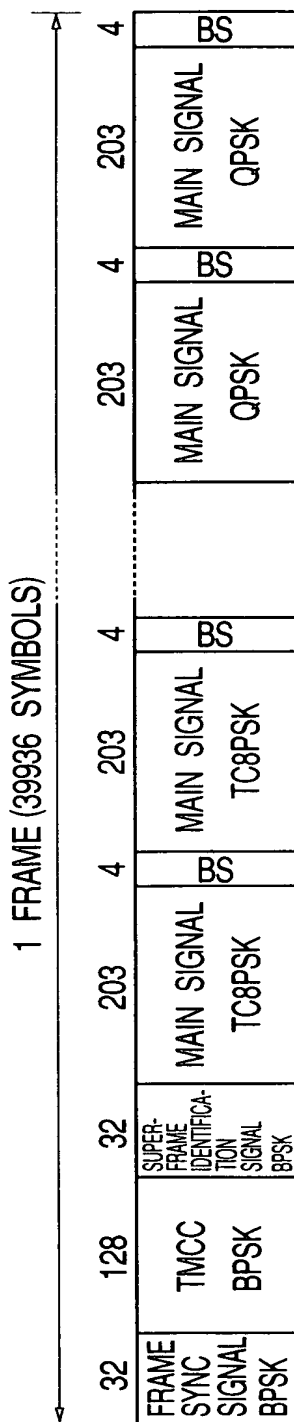
FIG. 7



The diagram illustrates a digital baseband processor for a digital video system, organized into several functional blocks and sections:

- Input and Initial Processing:** The process begins with an **IF** (Intermediate Frequency) input signal. This signal is split into two paths: one through a **90° PHASE SHIFTER** (12) and another through a **VCO** (11). The output of the phase shifter is mixed with the IF signal in a multiplier (60) to produce **I(8)**. The output of the VCO is mixed with the IF signal in a multiplier (61) to produce **Q(8)**.
- Filtering and Sampling:** The **I(8)** and **Q(8)** signals pass through **DIGITAL FILTER** blocks (62, 63) and **THINNING CIRCUIT** blocks (64, 65). These are then sampled by **A/D** converters (66, 67) to produce **i(1)** and **q(1)** signals.
- Carrier Reproduction Circuit 100:** This section is responsible for generating the carrier signals. It includes a **SELECTOR** (13) that receives **CLKSYB** (subcarrier clock) and **DM** (demodulation) signals. The selector outputs **14-1** to a **PHASE ERROR TABLE** (15-1) and **16D** to a **D/A** (17). The **D/A** output is filtered by an **LPF** (18) and then fed into the **VCO** (11). The **VCO** output is also fed into a **SELECTOR** (19) which produces **AR(3)** and **R(3)** signals.
- Frame Sync Signal Section:** This section contains a **REPRODUCTION FRAME SYNC SIGNAL** block (99) and a **FRAME SYNC SIGNAL SECTION SIGNAL** block (8F). The **REPRODUCTION FRAME SYNC SIGNAL** block includes a **BINARY CONVERTER** (101) and two **DELAY CIRCUIT** blocks (91). The **FRAME SYNC SIGNAL SECTION SIGNAL** block includes a **SELECTOR** (103) and an **ADDER** (102).
- Remapping and Averaging:** The **REMAPPER** block (7) takes **i(1)** and **q(1)** as inputs and produces **I'(8)** and **Q'(8)** signals. The **ADDER** (102) also receives **R(3)** and **AR(3)** signals. The output of the adder is fed into an **AVERAGING CIRCUIT** (95).
- Transmission Configuration Identification Circuit:** This block (9) receives **I'(8)** and **Q'(8)** signals and provides feedback to the **FRAME SYNC SIGNAL SECTION SIGNAL** block (8F).

PHASE ROTATION ANGLE JUDGEMENT CIRCUIT 92F



CLK_{SYB}

FIG. 10

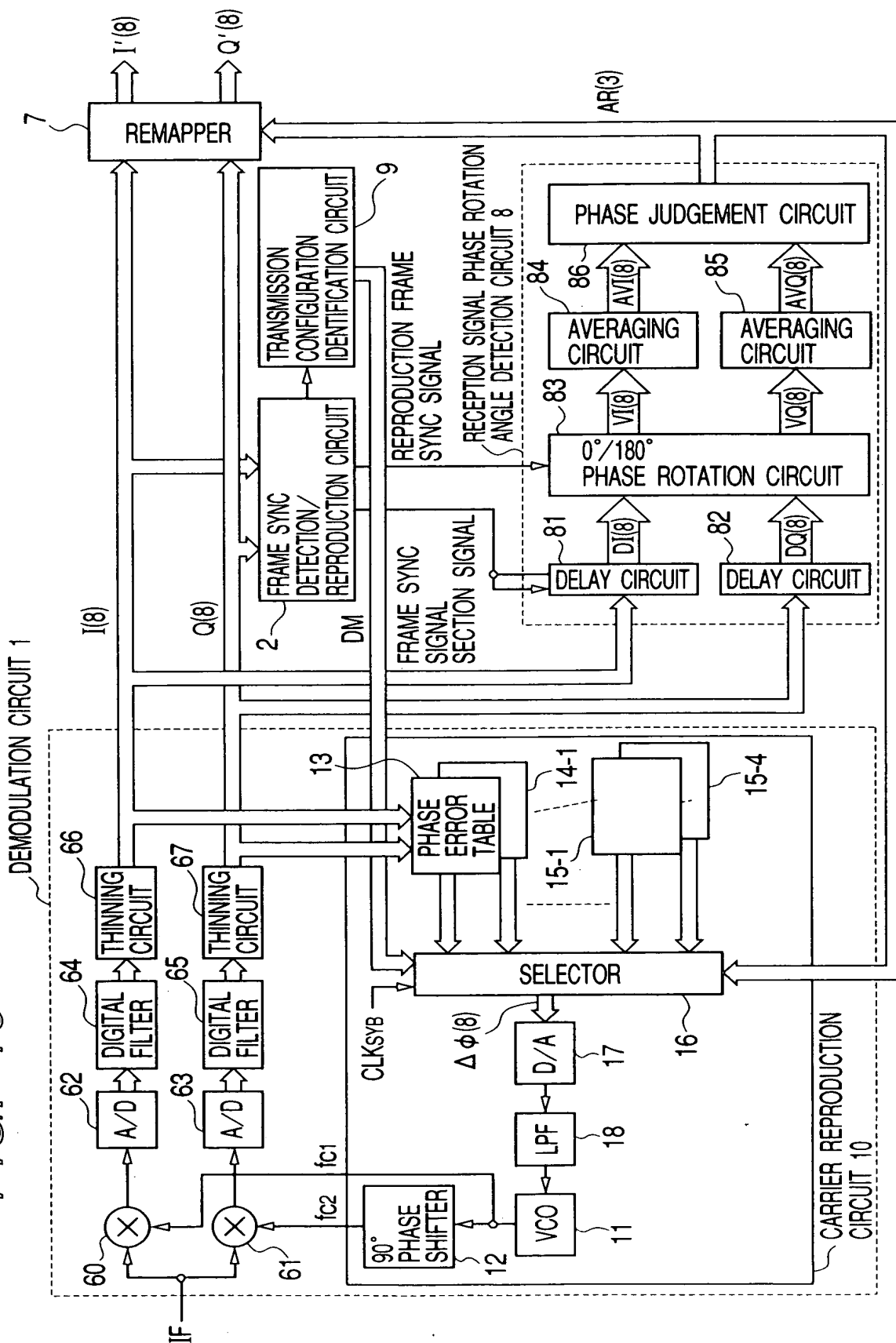


FIG. 11A

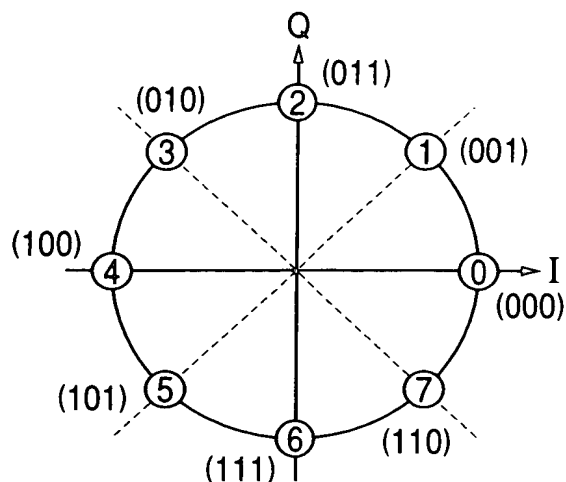


FIG. 11B

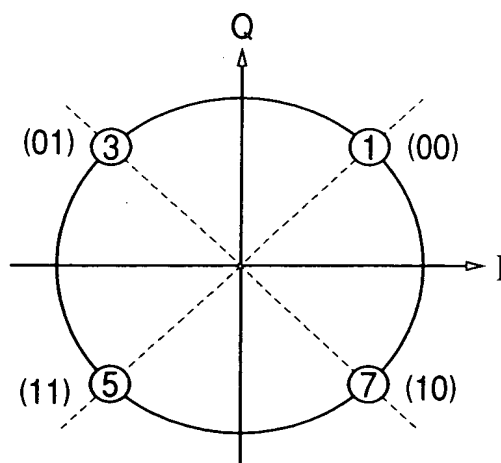
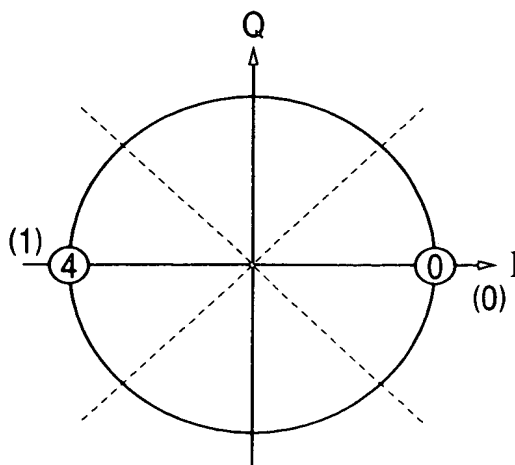


FIG. 11C



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FIG. 12

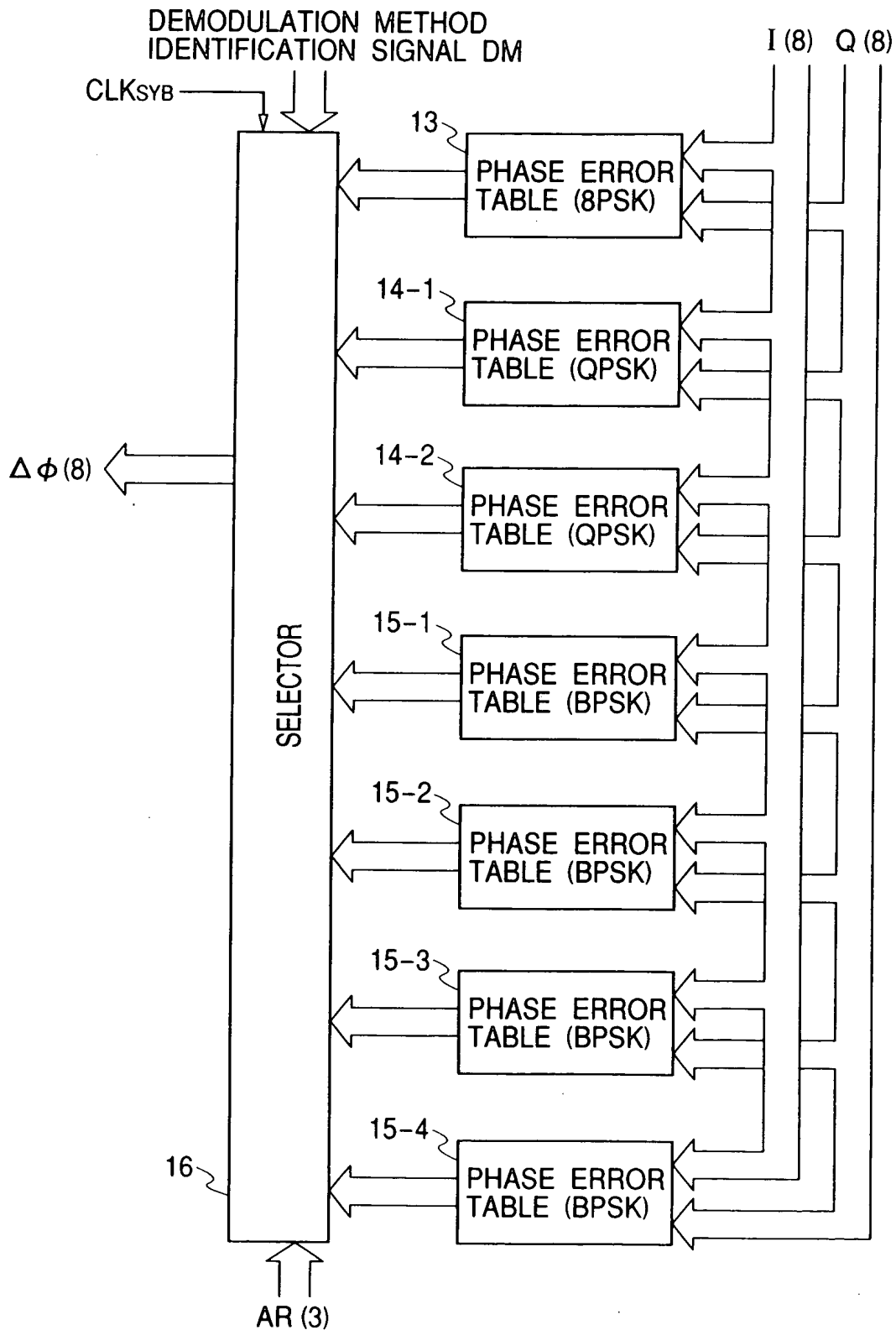


FIG. 13

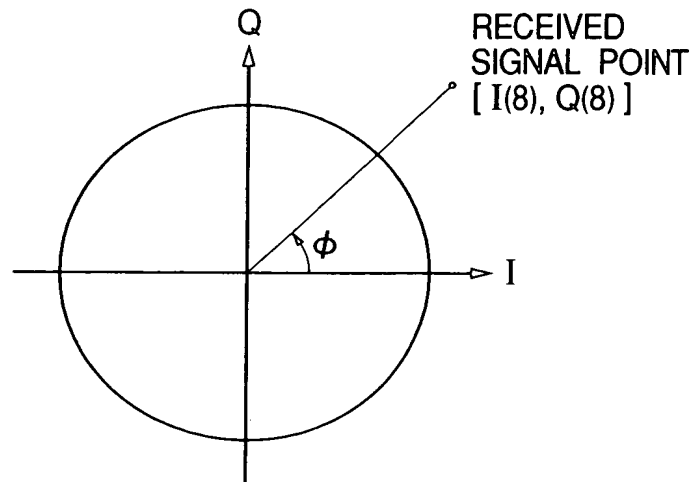
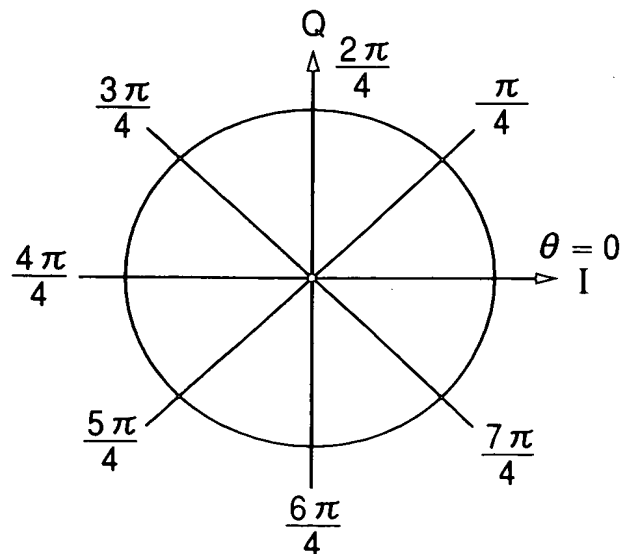


FIG. 14



[illegible]

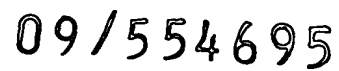


FIG. 17

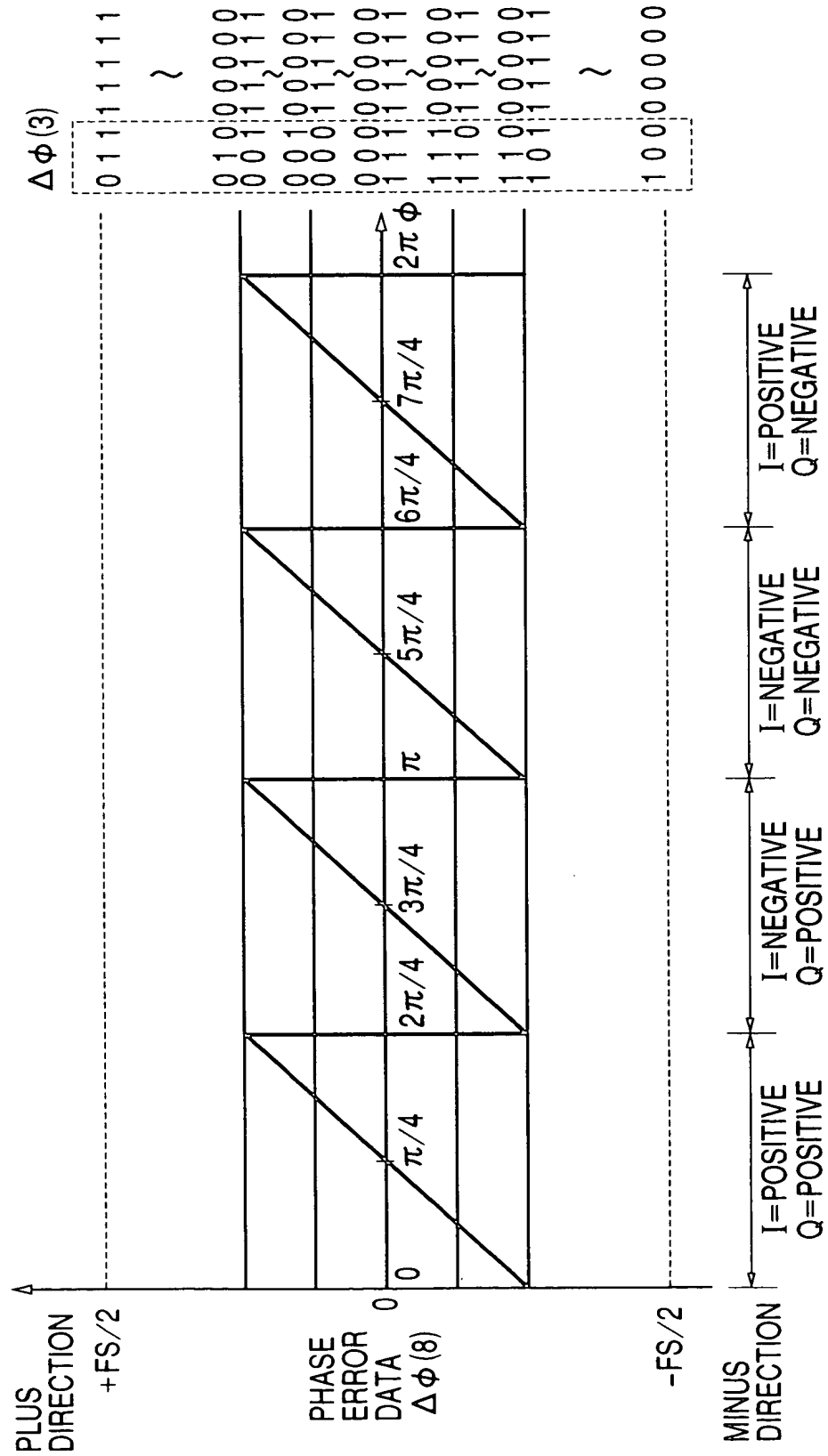
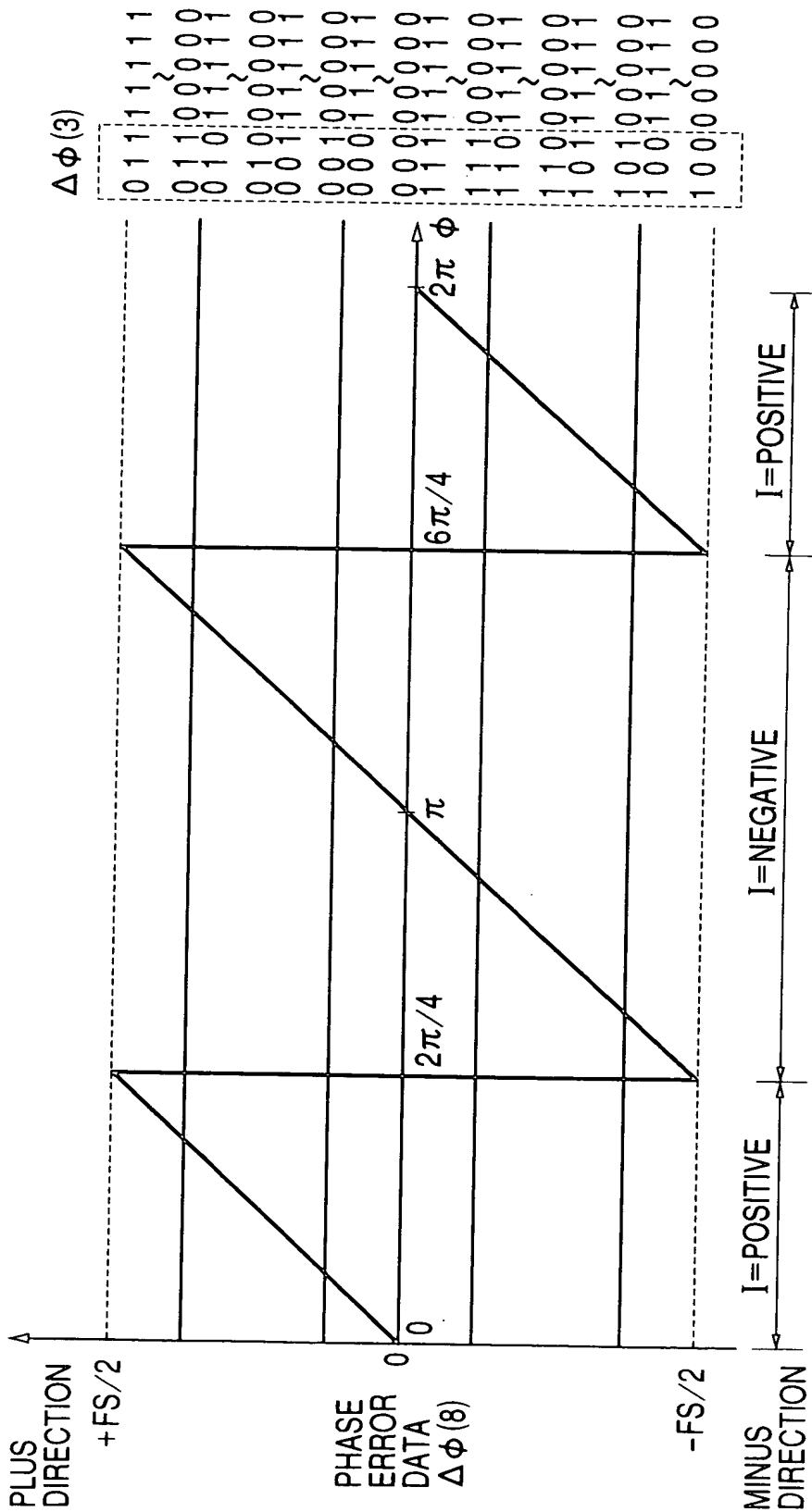


FIG. 18



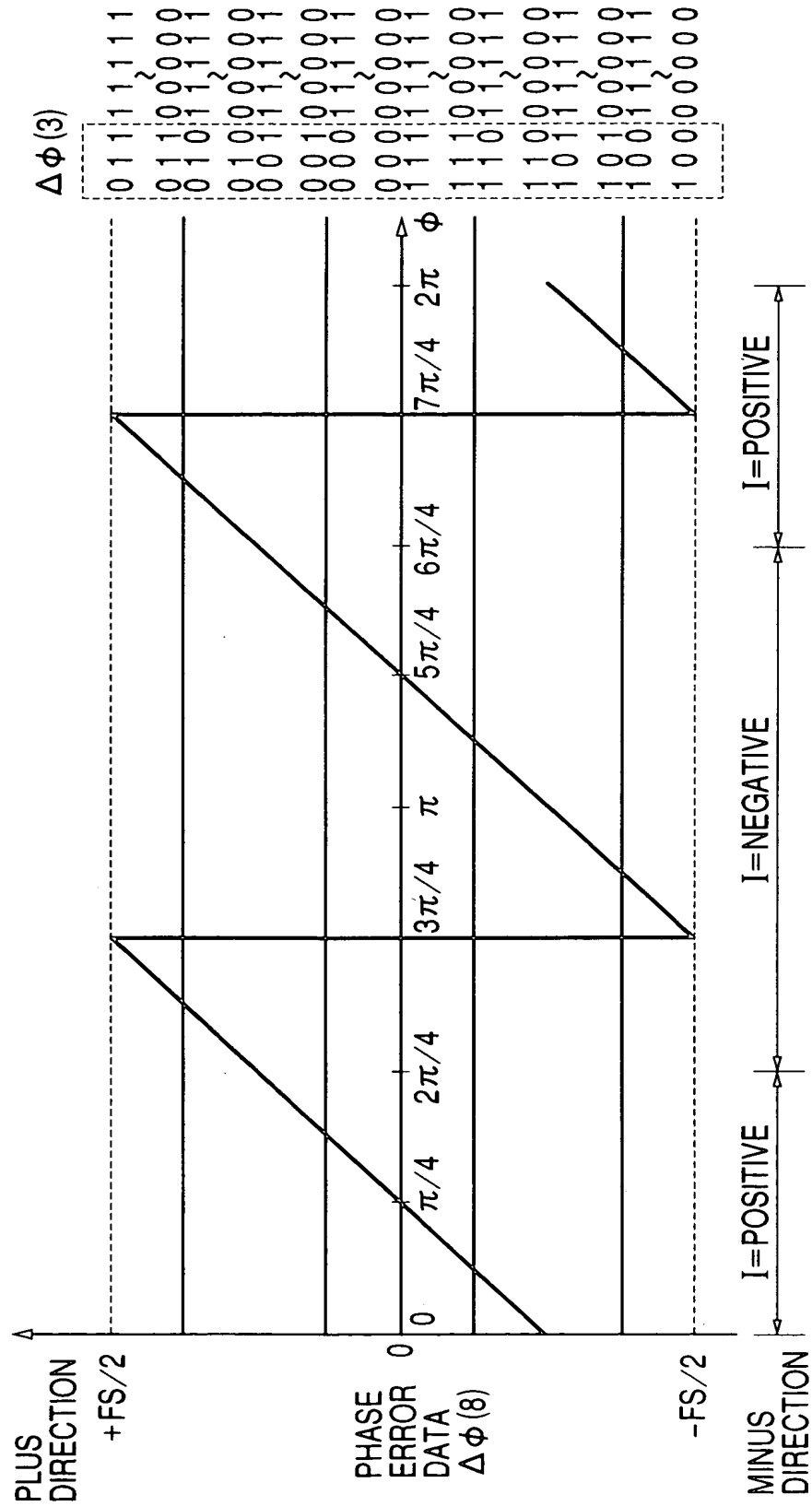
[illegible]

FIG. 20

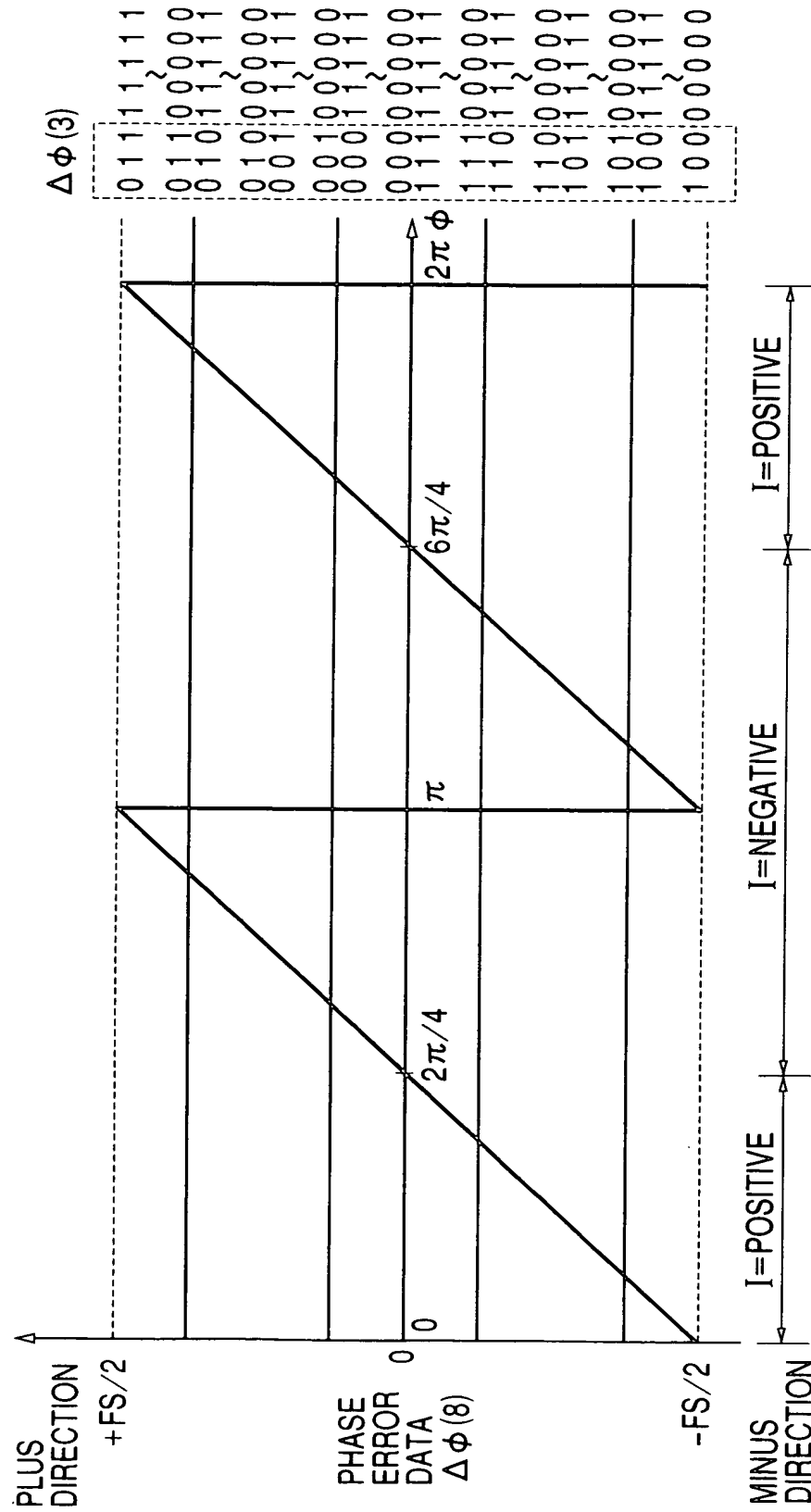


FIG. 21

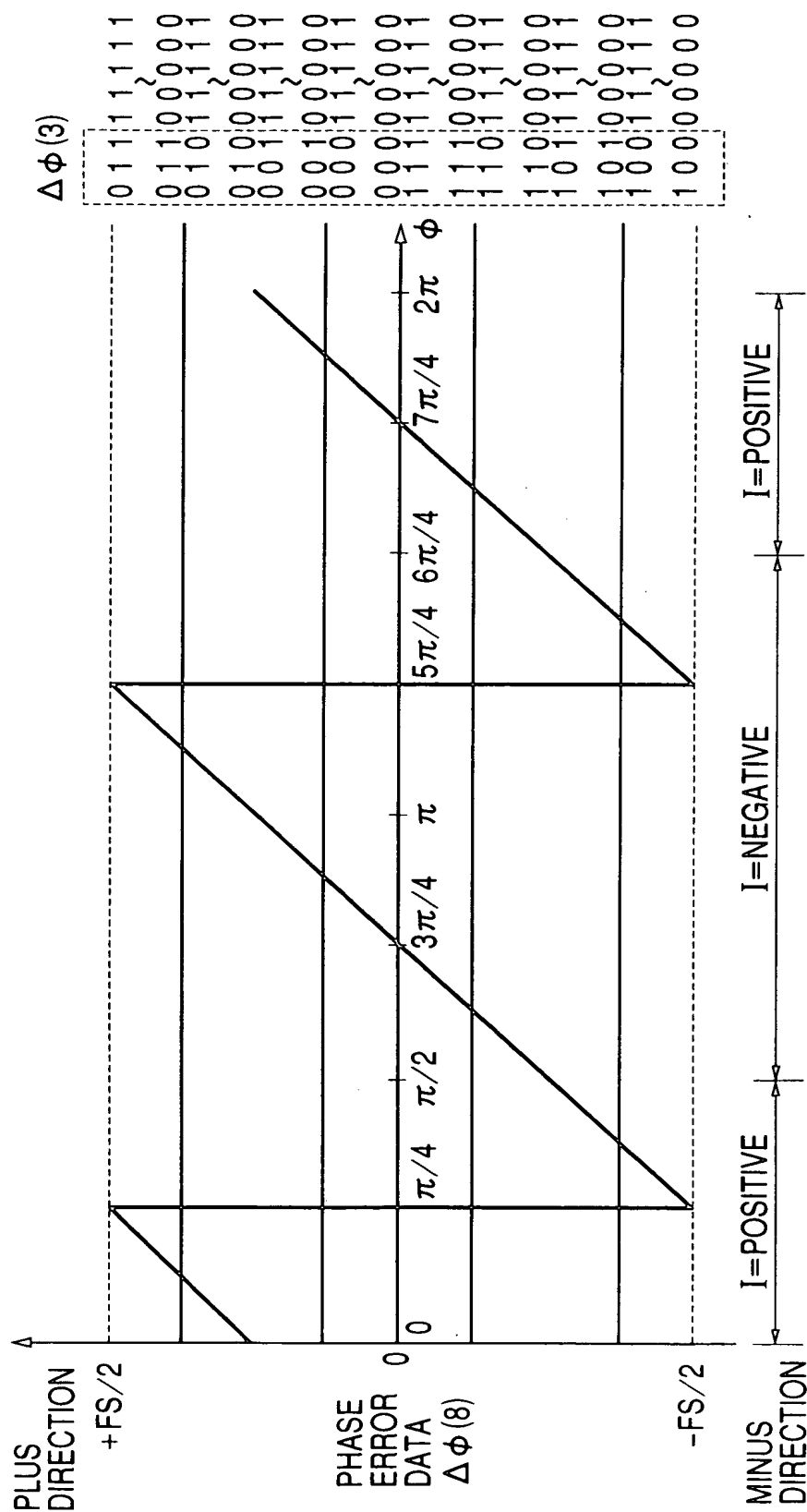


FIG. 22

FRAME SYNC DETECTION/REPRODUCTION CIRCUIT 2

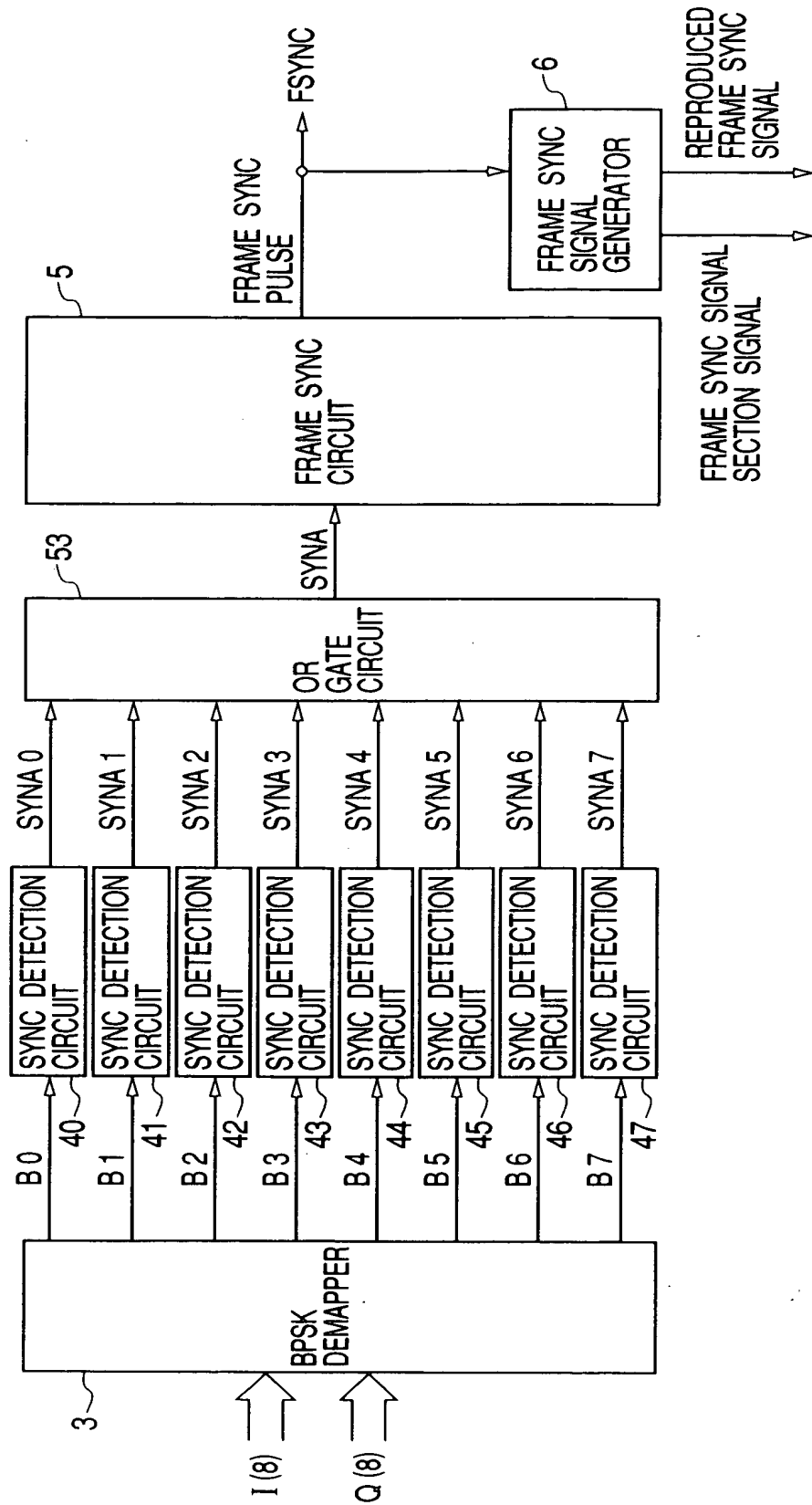


FIG. 23A

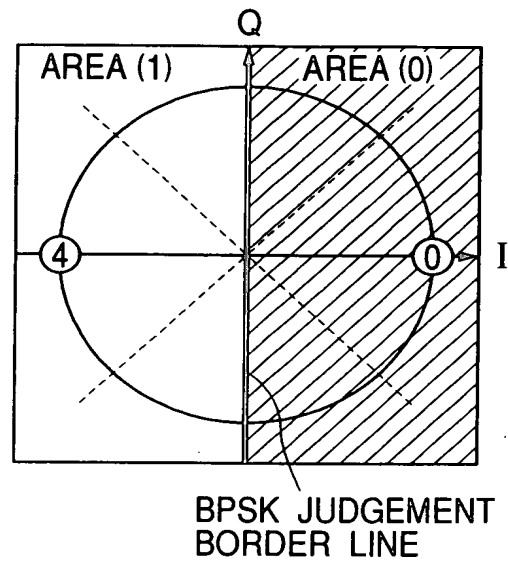


FIG. 23B

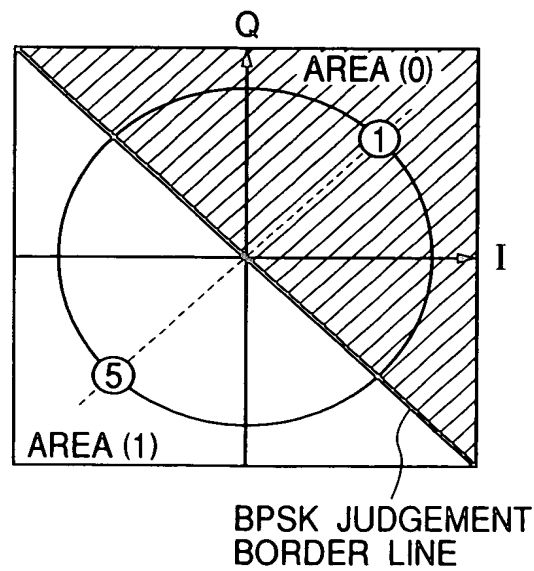


FIG. 24

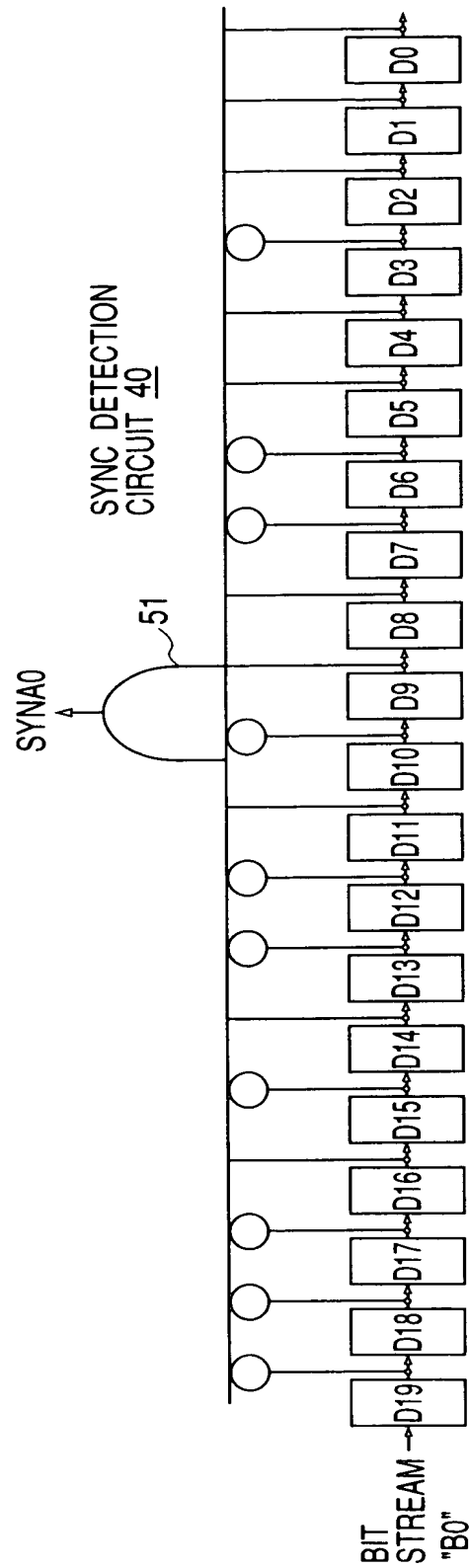


FIG. 25

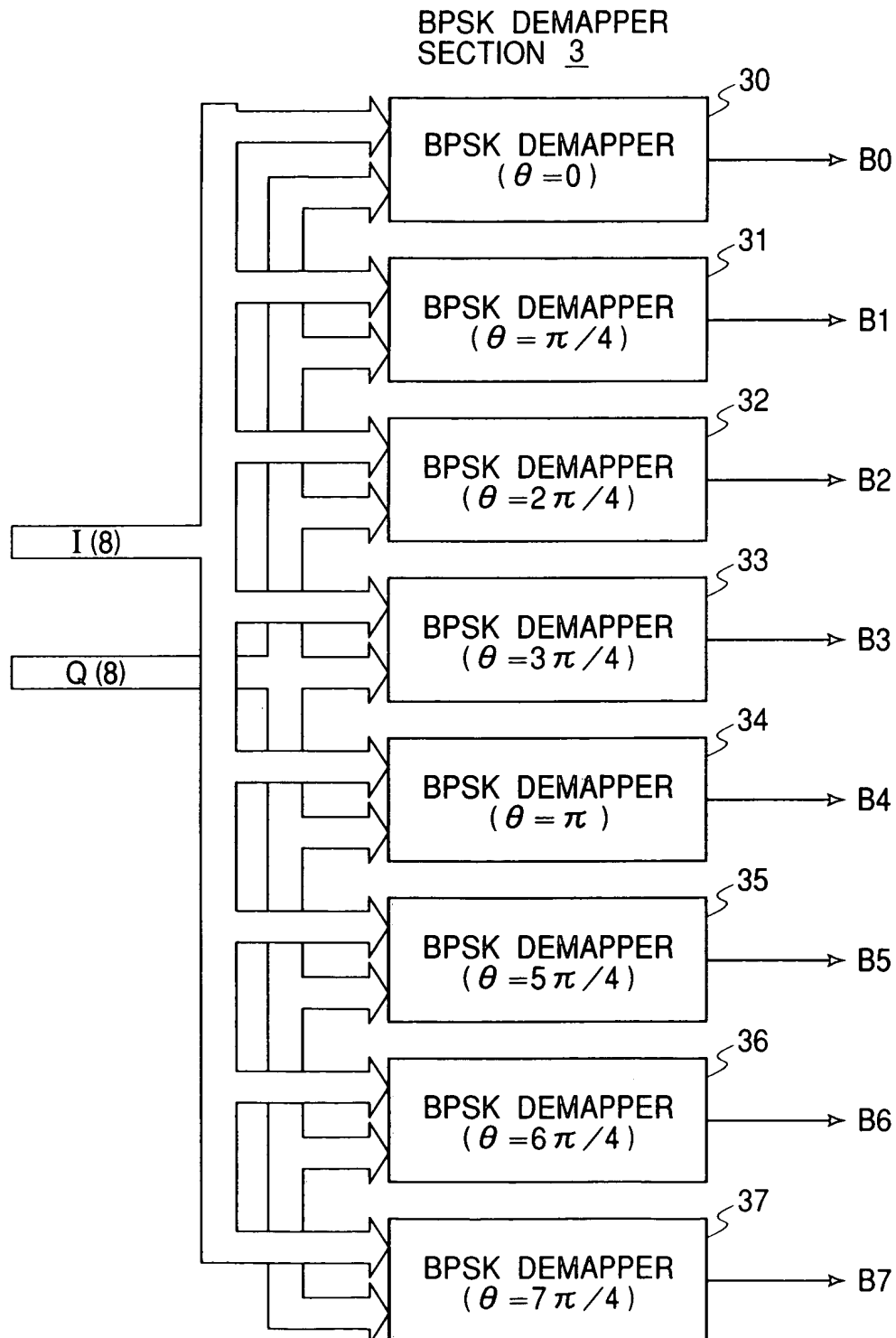


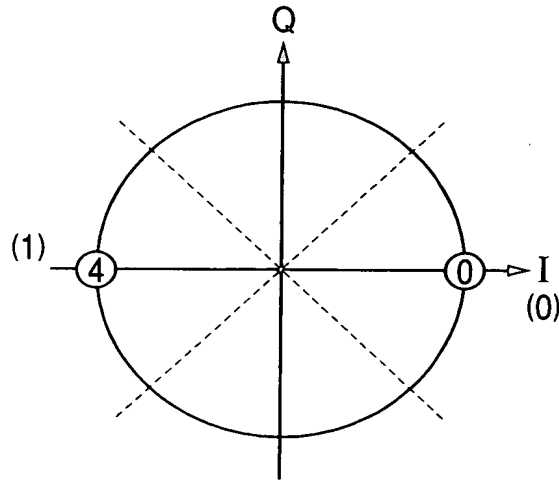
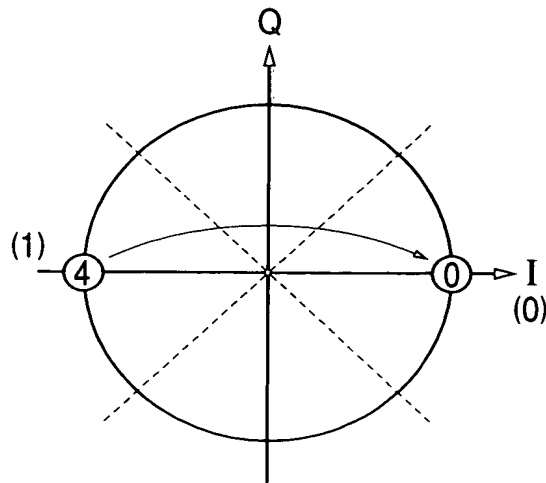
FIG. 26A*FIG. 26B*

FIG. 27

